IN THE CLAIMS:

1-14. (Canceled without prejudice or disclaimer)

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15.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion having one surface for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion, said inner lead portions of said plurality of leads being electrically connected with said bonding pads of said semiconductor chip; and

(c) a resin member sealing said semiconductor chip, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip, and

wherein said one surface of said chip mounting portion is a surface on which burrs are not formed, during formation of said chip mounting portion.

16.(New) A semiconductor device according to Claim 15, wherein said burrs are formed when said lead frame is made by pressing.

Amended

17.(New) A semiconductor device according to Claim 15, wherein said chip mounting portion has a substantially circular form in a plane view.

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18.(New) A semiconductor device according to Claim 16, wherein said chip mounting portion has a substantially cross form in a plane view.

19.(New) A semiconductor device according to Claim 15, wherein said inner lead portions of said plurality of leads are electrically connected with said bonding pads of said semiconductor chip by a plurality of bonding wires.

20.(New) A semiconductor device according to Claim 19, wherein parts of said inner lead portions of said plurality of leads, to which said plurality of bonding wires are connected, are plated.

21.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) a lead frame having:

a chip mounting portion for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion,

(c) a plurality of bonding wires electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, each of said inner lead portions of said plurality of leads having one surface to which a corresponding bonding wire among said plurality of bonding wires is connected; and

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(d) a resin member sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein said one surface of said inner lead portion of each of said plurality of leads is a surface on which burrs are formed, said burrs being resultant from formation of said plurality of leads.

22.(New) A semiconductor device according to Claim 21, wherein a size of said chip mounting portion is smaller than that of said semiconductor chip.

23.(New) A semiconductor device according to Claim 21, wherein said burrs are formed when said lead frame is made by pressing.

24.(New) A semiconductor device according to Claim 22, wherein said chip mounting portion has a substantially circular form in a plane view.

25.(New) A semiconductor device according to Claim 22, wherein said chip mounting portion has a substantially cross form in a plane view.

26.(New) A semiconductor device comprising:

(a) a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

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(b) a lead frame having:

a chip mounting portion having a first surface for mounting said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at a periphery of said chip mounting portion;

(c) a plurality of bonding wires electrically connecting said inner lead portions of said plurality of leads with said bonding pads of said semiconductor chip respectively, each of said inner lead portions of said plurality of leads having a second surface to which a corresponding bonding wire among said plurality of bonding wires is connected; and

(d) a resin member sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads,

wherein a size of said chip mounting portion is smaller than that of said semiconductor chip,

wherein said first surface of said chip mounting portion is a surface on which burrs are not formed, and

wherein said second surface of said inner lead portion of each of said plurality of leads is a surface on which said burrs are formed, said burrs resultant from formation of said chip mounting portion and said plurality of leads.

27.(New) A method of manufacturing a semiconductor device, comprising the steps of:

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(a) preparing a semiconductor chip having a plurality of semiconductor elements and bonding pads formed on a main surface thereof;

(b) preparing a lead frame having:

a chip mounting portion having one surface for mounting said semiconductor chip, a size of said chip mounting portion being smaller than that of said semiconductor chip; and

a plurality of leads each having an inner lead portion and an outer lead portion continuously formed with said inner lead portion and being arranged at the periphery of said chip mounting portion, wherein said one surface of said chip mounting portion is a surface on which burrs are not formed, said burrs resultant from formation of said chip mounting portion by pressing;

(c) after the step (b), mounting said semiconductor chip on said one surface of chip mounting portion;

(d) electrically connecting said inner lead portions of said plurality of leads with said bonding wires of said semiconductor chip by a plurality of bonding wires respectively; and

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(e) sealing said semiconductor chip, said plurality of bonding wires, said chip mounting portion and said inner lead portions of said plurality of leads.